REMARKS/ARGUMENTS

Claims 8-17 and 23-25 are pending, claims 14, 15, 17, and 24 are amended, and claims 18-21 are canceled.

Claims 14 and 15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with enablement requirement, and under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships. Claim 14 is amended to recite ". . . the data and clock recovery circuit further comprises a serial-parallel converter and a memory element having a look-up table stored therein, and the data and clock recovery circuit serial-parallel converts the electrical signals and compares the converted signals with data in the looked-up table . . .." Also, FIG. 2 is amended to depict the serial-parallel converter (50) and the memory element (52) which are described on page 5 of the specification. No new matter is added. It is respectfully submitted that claims 14 and 15 are now patentable in view of 35 U.S.C. 112, first and second paragraphs, therefore, withdrawal of the above rejections are respectfully requested.

The drawings are objected to because the serial-parallel converter and the memory element must be shown. Again, FIG. 2 is amended to depict the serial-parallel converter (50) and the memory element (52) which are described on page 5 of the specification. Page 5 of the specification has also been amended to incorporate reference numerals from the amended drawing. No new matter is added. Accordingly, Applicant

respectfully requests that the above-mentioned objection be withdrawn.

Claims 8, 9, 12 and 13 are rejected under 35 U.S.C. 102(e) as being fully anticipated by Bala et al. (6,272,154); claim 11 is rejected under 35 U.S.C. 103(a) as being obvious over Bala et al.; claims 10, 16, 17 and 18 are rejected under 35 U.S.C. 103(a) as being obvious over Bala et al., in view of Johnston, Jr (6,101,204); claims 19, 20 and 21 are rejected under 35 U.S.C. 103(a) as being obvious over Bala et al., in view of Yoo (6,519,062); claim 23 is rejected under 35 U.S.C. 103(a) as being obvious over Kuroyanagi et al. (6,433,900), in view of Bala et al.; and claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being obvious over Kuroyanagi et al., in view of Bala et al. Applicant submits that all of the claims currently pending in this application are patentably distinguishable over the cited references, and reconsideration and allowance of this application are respectfully requested.

The independent claim 8 includes, among other limitations, "a data and clock recovery circuit for recovery of data and corresponding clocking information from the corresponding electrical signal and outputting said data as a respective recovered electrical signal, said data and clock recovery circuit recovering data streamed at multiple different clock rates and multiple different protocols."

Bala does not disclose the above-recited limitation. Rather, Bala in the cited text (col. 4, lines 15 to 20) states "[a]s shown in FIG. 1, the network element 102 may include

demultiplexers 108 to extract an optical service channel (OSC) signal from the input fibers of the transfer interfaces 104a, 104b. For example, the OSC signals may be provided at 1510 nm. The OSC signals are connected to input ports on an asynchoronous transfer mode (ATM) switch 110 or any other protocol that may be used on the OSC. Similarly, the network elements 102 may include multiplexers 109 to add OSC signals from the ATM switch 110 to the output fibers of the transfer interfaces 104a, 104b." (Id.).

Applicant respectfully submits that there is no support in Bala for the assertion in the Office action that a data and clock recovery circuit recovers data streamed at multiple different protocols. Instead, Bala discloses an optical service channel (OSC) extracted by demultiplexers 108 from the input fibers of the transfer interfaces 104a, 104b. With further reference to Figures 1 and 2 of Bala, the OSC signals are extracted before demultiplexers, e.g., 216a. Accordingly, it would be clear to a person skilled in the art that data and clock recovery on the respective individual signal channels can only be performed after demultiplexing. Thus, the OSC signals in Bala are not subjected to processing by the CDR units, e.g,. 254, 235. This is confirmed by the connectivity of the extraction/addition points, e.g., 217 and 237 in Figure 2.

In relation to disclosure of data and clock recovery of the extracted OSC signals, Bala states "…The OSC signals are connected to input ports on an asynchoronous transfer mode (ATM) switch 110 or any other protocol that may be used on the OSC…,"

as mentioned above. Applicant respectfully submits that, to a person skilled in the art, this, at best, suggests that any processing is performed according to the one protocol used in the OSC. In other words, there is no disclosure of any reconfigurability to different protocols in Bala. This is in contrast to providing a "multi-protocol" capability for the OSC signal processing, according to the presently claimed invention.

The Office action further refers to col. 6, lines 40 to 50 of Bala for supporting that Bala discloses extracting signal information used for signal processing at multiple different clock rates and multiple different protocols and performance monitoring. The relevant disclosure in Bala referred to clearly states: "For example, the CDR circuitry 254 may perform clock and data recovery functions for signals at OC-48, OC-12, or OC-3 data rates. For SONET OC-48 signals, the CDR circuitry 254 may also monitor the J0 and B1 bytes of the SONET overhead data, both before and after the cross-connect, providing information on the identify and bit error rate (BER) of each such signal, and confirming the operation of the cross-connect. Opto-electric transmitters 258 convert the electronic signals received from the cross-connect switches 255 to optical signals, for example, at 1.3 μm. The signals to be dropped are coupled to the client-drop ports 265".

Importantly, Applicant respectfully submits that it is clear to a person skilled in the art that OC-3, OC-12, OC-48 are all <u>one</u> protocol derived from multiplexing 3, 12 and 48 STS-1s respectively. Each of these signals is managed exactly in the

same fashion, for example using B1 bytes, which are common to OC-3, OC-12, and OC-48 (see above). Therefore, Applicant respectfully submits that there is no disclosure of a multi protocol signal processing and performance monitoring in the cited prior art. A "multi-rate" CDR, as disclosed in Bala, is inherently not capable of synchronising to other protocols. As specifically disclosed in col. 10, lines 54 to 56, the CDR circuits are by-passed for signals other than OC-48, OC-12, and OC-3. Consequently, independent claim 8 is not anticipated by Bala. Likewise, none of the remaining cited references, alone or in combination, teach or suggest the above discussed limitation of claim 8. Therefore, claim 8 is allowable over the cited references.

Dependent claims 9-16 are dependent from claim 8 and therefore include all the limitations of claim 8 and additional limitations therein. Accordingly, these claims are also not anticipated by Bala, as being dependent from allowable independent claim 8 and for the additional limitations they include therein.

Similarly, the remaining independent claims 17 and 23-25 include the above-mentioned limitation. Thus, for the same reasons discussed above, these claims are also allowable over the cited references.

In view of the foregoing amendments and remarks, it is respectfully submitted that this application is now in condition for allowance, and accordingly, reconsideration and allowance are respectfully requested.

Respectfully submitted,
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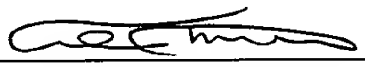
By 
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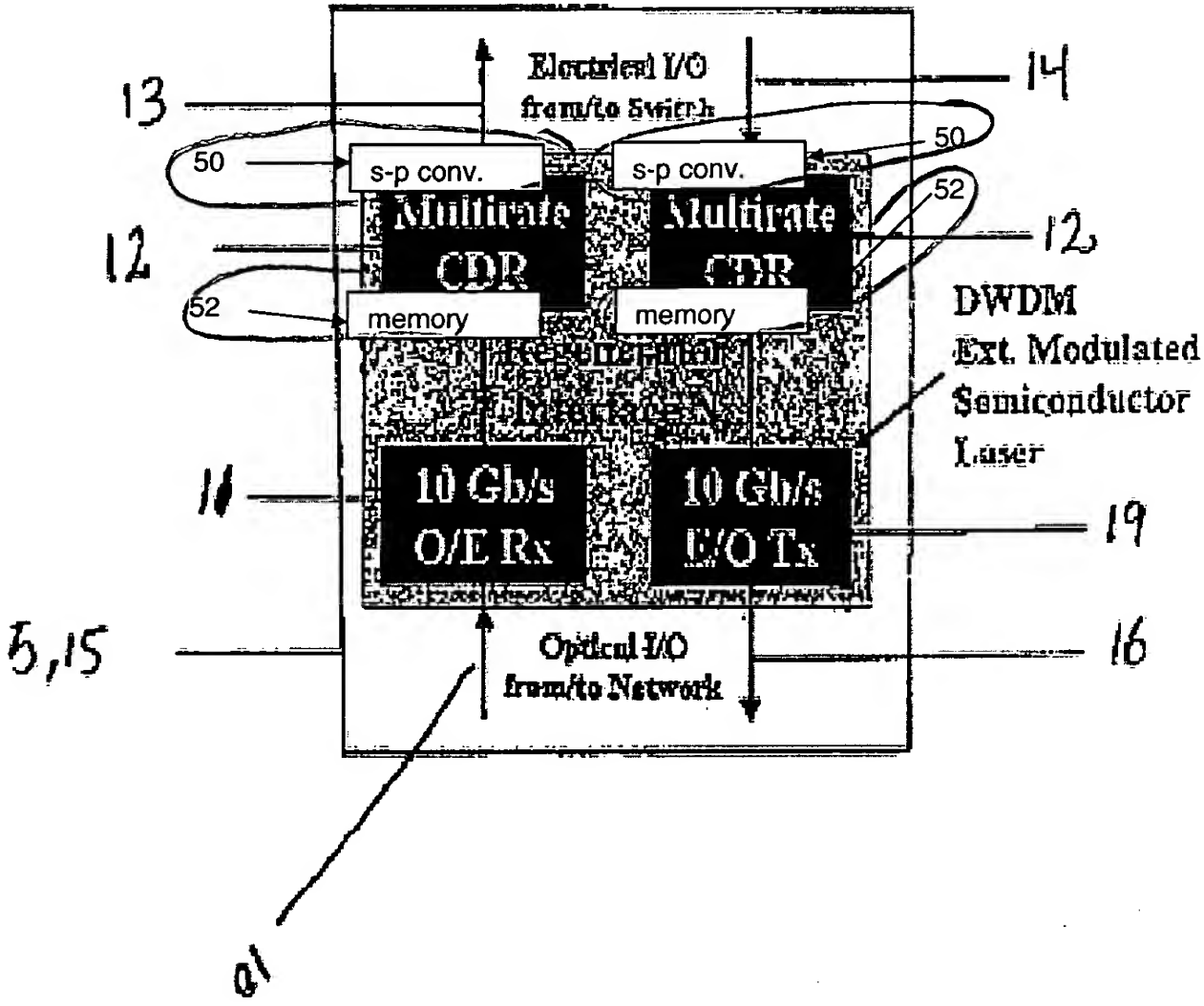

FIG. 2